REMARKS

Claims 1-2, 4, 7-8, 10-11, 13, 16-17, 20-21 and 24 have been rejected under 35 U.S.C. 102(e) as being anticipated by Abdallah et al. (U.S. 6,377,970), and claims 3, 5, 12, 14, 19 and 23 have been rejected under 35 U.S.C. 103(a) as being obvious over Abdallah et al., as applied to claim 1, in view of Cheung et al. (U.S. 6,369,610). Similarly, claims 6, 9, 15, 18 and 22 have been rejected under 35 U.S.C. 103(a) as being obvious over Abdallah et al., as applied to claim 1, in view of Aldrich et al. (U.S. Patent 6,601,077). These rejections are respectfully disagreed with, and are traversed below.

Claim 1 is directed to a data processor, comprising:

> "a multiplier block having a multiplier front end for generating partial products from input operands; and a plurality of arithmetic logic units (ALUs) having inputs switchably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being switchably coupled, in a second mode of operation, to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources" (emphasis added).

Independent claim 21 is directed to a digital signal process (DSP), comprising:

> "a DSP core having a register file, at least one arithmetic logical unit (ALU), and at least one multiplier block comprised of a multiplier front end for generating partial products from input operands, and multiplier block further comprising circuitry for adding together said partial products, said circuitry comprising a plurality of ALUs having inputs that are programmably coupled, in a first mode of operation, to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, said inputs of said plurality of ALUs being programmably coupled, in a second mode of operation, to second data sources for selectively operating together in parallel for performing at least one arithmetic and logical operations on data received from said second data sources, wherein said partial products have a width of n-bits, and where a width of individual ones of said

plurality of ALUs is one of n-bits or less than n-bits.

Similarly, independent method claim 10 is directed to a method of operating a data processor, comprising:

> "providing a multiplier block having a multiplier front end for generating partial products from input operands; and
>
> providing said multiplier block with a plurality of arithmetic logic units (ALUs); wherein
>
> in a first mode of operation, said plurality of ALUs have inputs switchably coupled to first data sources comprised of outputs of said multiplier front end for adding together partial products received therefrom to arrive at a multiplication result; and
>
> in a second mode of operation, said inputs of said plurality of ALUs are switchably coupled to second data sources for performing at least one of arithmetic and logical operations on data received from said second data sources."

First, it is respectfully submitted that the newly cited Abdallah et al. reference relates to a completely different method and apparatus than that of the presently claimed invention, and one skilled in the art seeking to develop that which Applicant's claim would not be motivated to look for Abdallah et al. for guidance. For example, Abdallah et al. disclose a method and apparatus to reduce the amount of silicon area required to implement a packet sum of absolute differences (PSAD) instructions without increasing the time required to compute the PSAD (col. 2, lines 29-32). In this method, each of the first set of portions of partial products is produced using a first set of partial product selectors in multiple, with each of the first set of portions of the partial products being zero. Each of the multiple elements is inserted into one of the second set of portions of the partial products using a second set of partial products selectors, with each of the second of portions of the partial products being aligned. Additionally, each of the multiple elements are added together to produce the result including a field having a sum of the multiple elements.

Abdallah et al. do not disclose or suggest any first mode of operation where first data sources are

comprised of outputs of a multiplier front end for adding together partial products received therefrom to arrive at a multiplication result, and a second mode of operation performing at least one of arithmetic and logical operations on data received from said second data source.

The Examiner alleges that Applicant's "second mode" of operation is disclosed at col. 10, lines 10-15 of Abdallah et al. Applicant respectfully disagrees. In col. 9, line 59 to col. 10, line 15 of Abdallah et al., a CNTR2 is described as follows: when the CNTR2 signal is asserted, certain partial product selectors within set 16x16 multiplier are configured to insert each packet data element G_i into a portion of one of the first sixteen partial products. In contrast, according to Applicant's second mode of operation, at least one arithmetic and logical operations is performed on data received from said second data sources. This is not disclosed nor suggested by Abdallah et al.

The Examiner further appears to be of the position that Figures 11 and 12 of Abdallah et al. anticipate Applicant's independent claims. Applicant respectfully disagrees and points out that the PADDH apparatus 1150 is for executing a Packed Add Horizontal instruction (see col. 5, lines 62-63). The Examiner appears to be equating the Carry Save Adder with Carry Lookahead Adder trees 1120 and 1110 with a plurality of ALUs having inputs switchably coupled to different data sources. Applicant respectfully fails to see the basis for this position and asserts that there is no teaching or suggestion in Abdallah et al., which would motivate one skilled in the art to arrive at the present claims.

For at least the foregoing reasons, it is respectfully submitted that Abdallah et al. do not disclose or suggest the presently claimed invention.

Applicant's further assert that the addition of Aldrich et al. and/or Cheung et al. does not cure the shortcomings of Abdallah et al. Turning first to Aldrich et al., what is disclosed therein appears to be a multi-state (three stage) pipelined processing unit optimized for pixel processing, more specifically one optimized for performing sum of absolute difference (SAD) calculations for pixel pairs (see col. 3, lines 10-40). In the embodiments of Figs. 2, 3, 4 and 5 it appears that the

pixel pair SAD values are computed in the first stage, they are combined in the second stage, and the third stage accumulates these combined values over an image frame.

Although it is not admitted that there is any suggestion in the reading of Aldrich et al. and Abdallah et al. that they could be combined in the manner done by the Examiner, it is asserted that if one were to make the combination, the resulting modified system would still suffer from the shortcomings of the Abdallah et al. system, as described above. Further, it is not seen where Aldrich et al. cure these shortcomings by teaching or suggesting, as in Applicant's claimed invention, that a plurality of ALUs have inputs switchably coupled, in a first mode of operation, to first data sources comprised of outputs of a multiplier front end for adding together partial products or, in a second mode of operation, to second data sources for performing at least one of arithmetic and logical operations on data received from the second data sources. Similarly, the addition of Cheung et al., which is directed to a reconfigurable multiplier array, does not disclose or suggest these features.

Applicant further respectfully points out that, in contrast to the cited references, an advantage of aspects of the presently claimed invention is in providing a DSP wherein a multiplier front end comprises at least one configurable ALU, where the ALU is employed for accumulating partial results during MAC operations (multiplication results) and may also be used as one or more ALUs during non-MAC operations (arithmetic and/or logical operations). According to aspects of the claimed invention, the ALUs inputs are switchably or programmably coupled. In a first mode, the ALUs inputs are coupled to first data sources and in the second mode ALUs inputs are coupled to second data sources (see independent claims 1, 10, 21 and page 4, lines 1-4 and 16-25 of the specification). A further advantage is that the plurality of ALUs can operate together in parallel.

It is respectfully submitted that independent claims 1, 10 and 21 are all patentably distinct from Abdallah et al. and the Examiner's proposed combination of this patent with either Aldrich et al. or Cheung et al. Since this is true, then all of the dependent claims are patentable as well, at least for the reason that each depends either directly or indirectly from an allowable independent

claim.

The Examiner is respectfully requested to reconsider and remove the rejections, and to allow the claims as presented above. An early notification of the allowance of claims 1-24 is earnestly solicited.

Respectfully submitted:

Christine Wilkes Beninati June 10, 2004

Christine Wilkes Beninati Date

Reg. No.: 37,967

Customer No.: 29683

HARRINGTON & SMITH, LLP
4 Research Drive
Shelton, CT 06484-6212

Telephone: (203)925-9400
Facsimile: (203)944-0245
email: cbeninati@hspatent.com

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. BOX 1450, Alexandria, VA 22313-1450.

6/10/04 Ann Okrentowich

Date Name of Person Making Deposit